

FIG. 16.2 is a schematic diagram of a memory array structure.

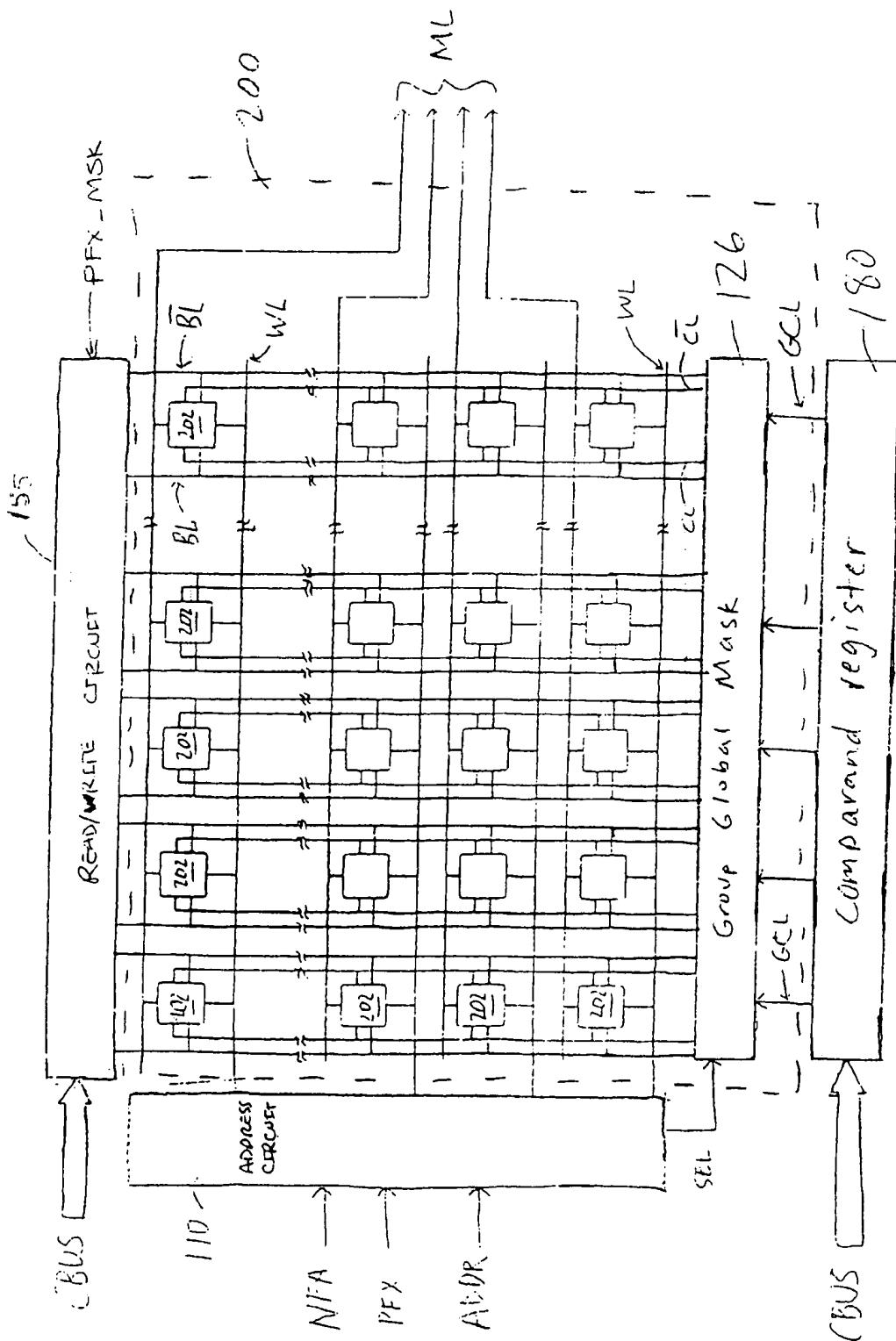


FIG. 2

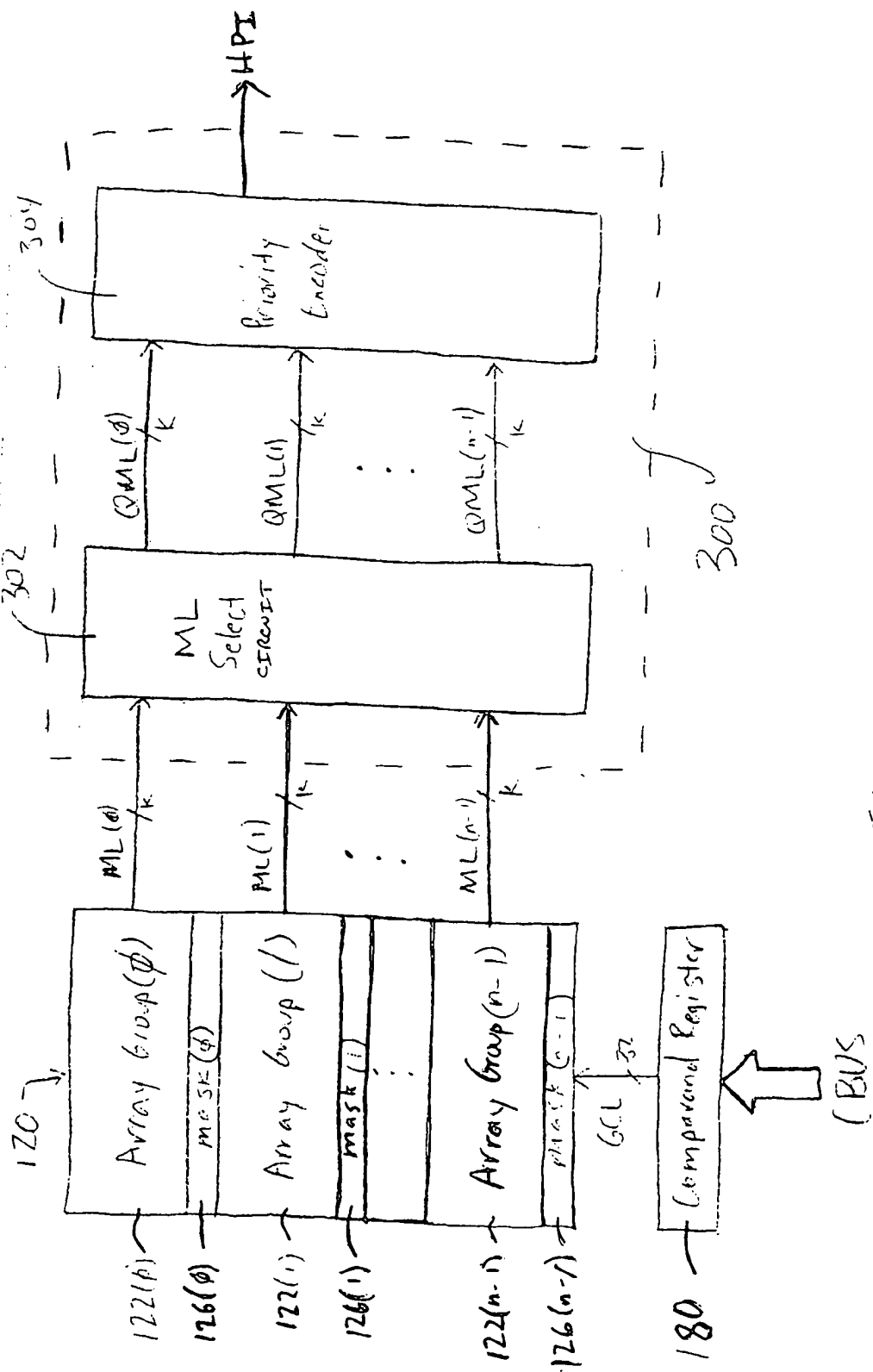


FIG. 3

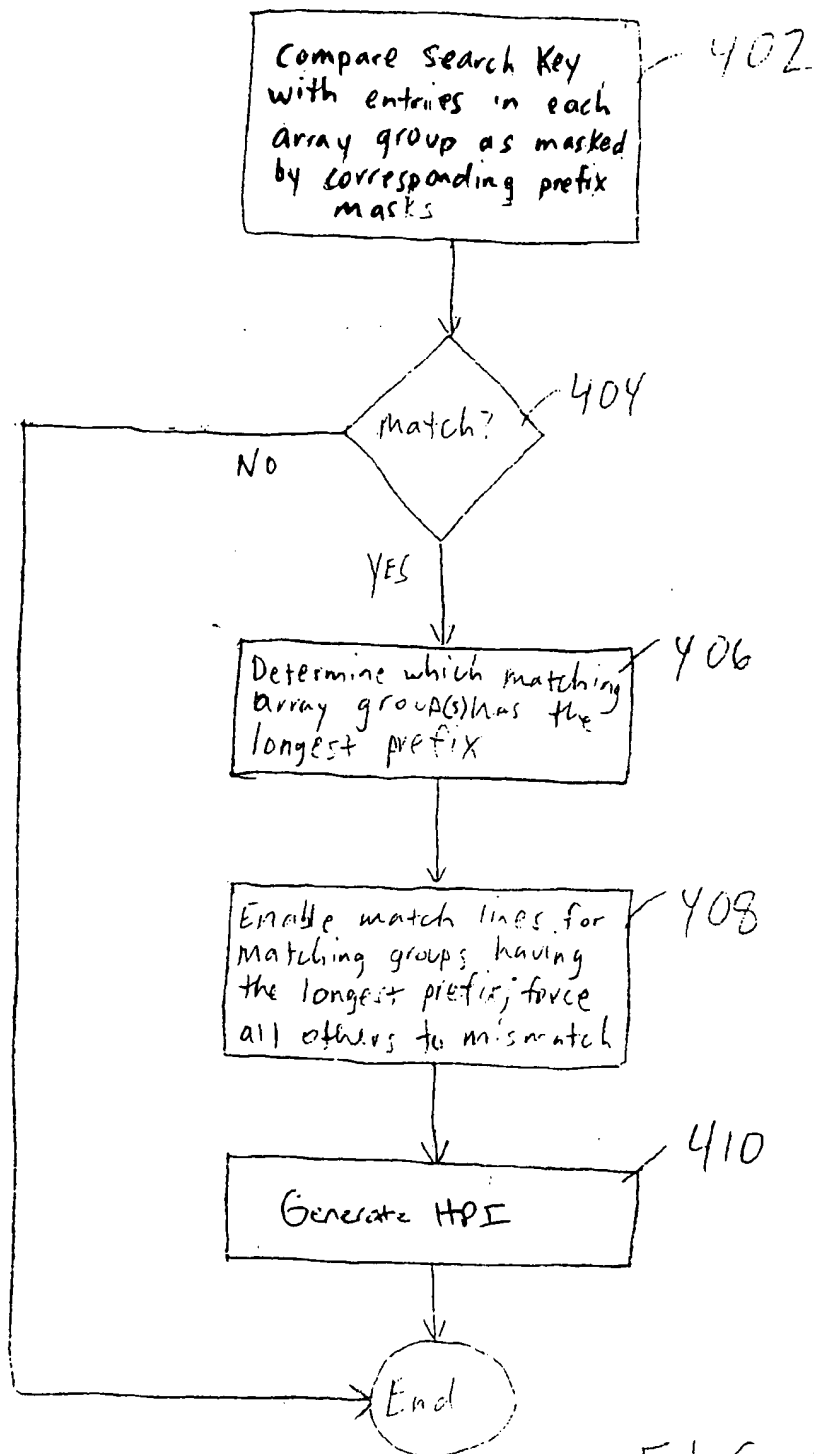


FIG. 4

FIG. 5A

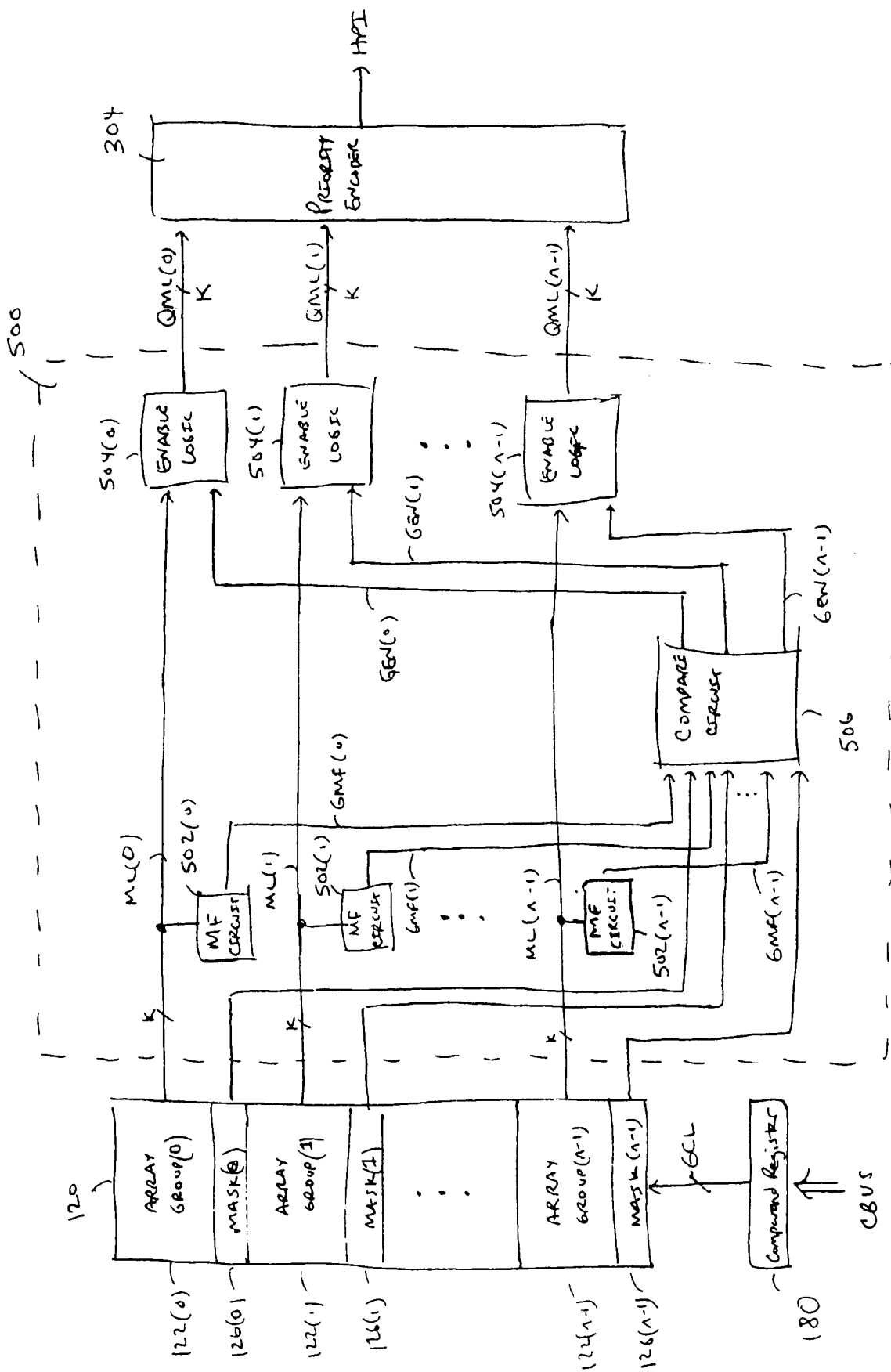


FIG. 5A

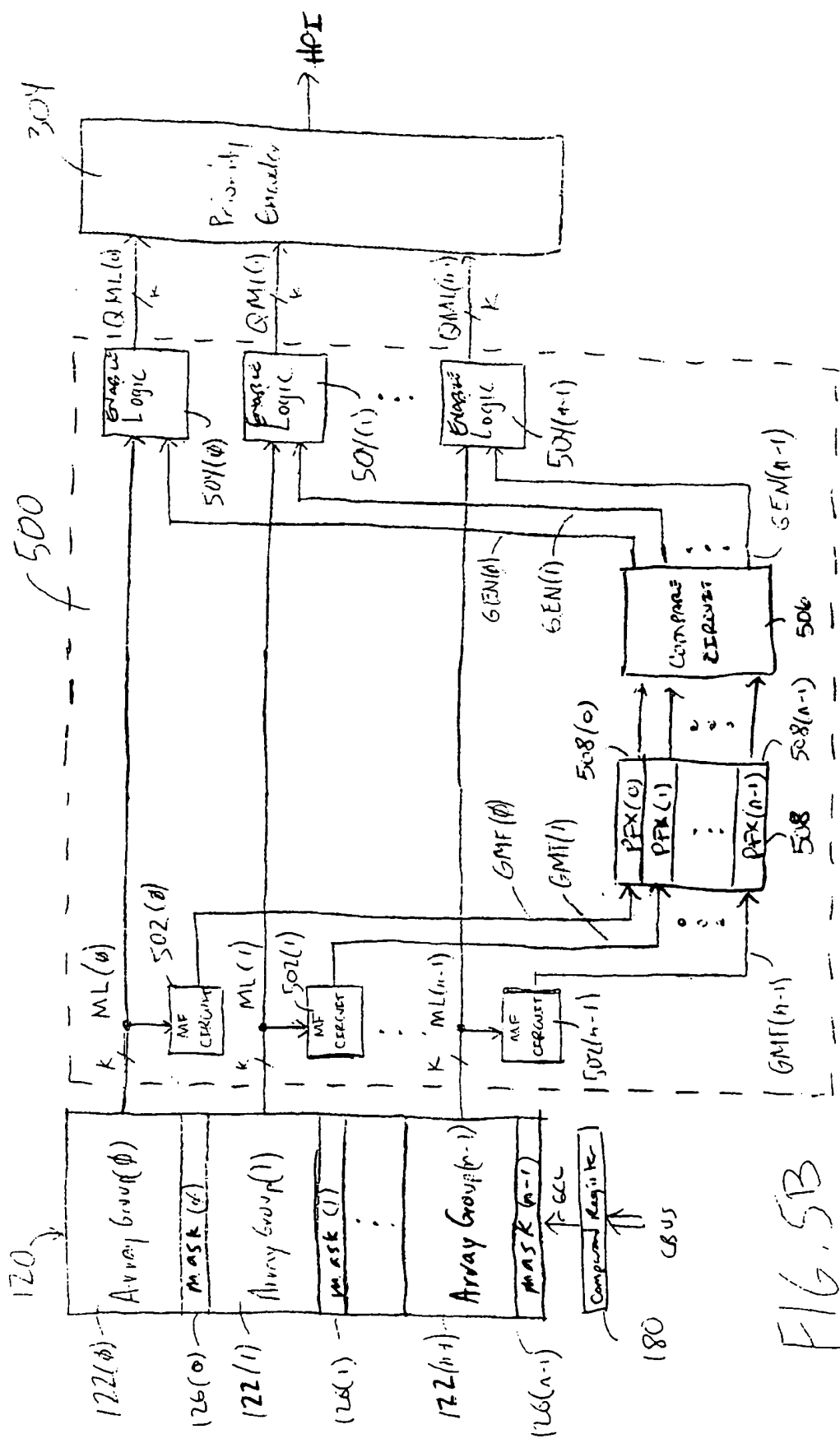


FIG. 5B

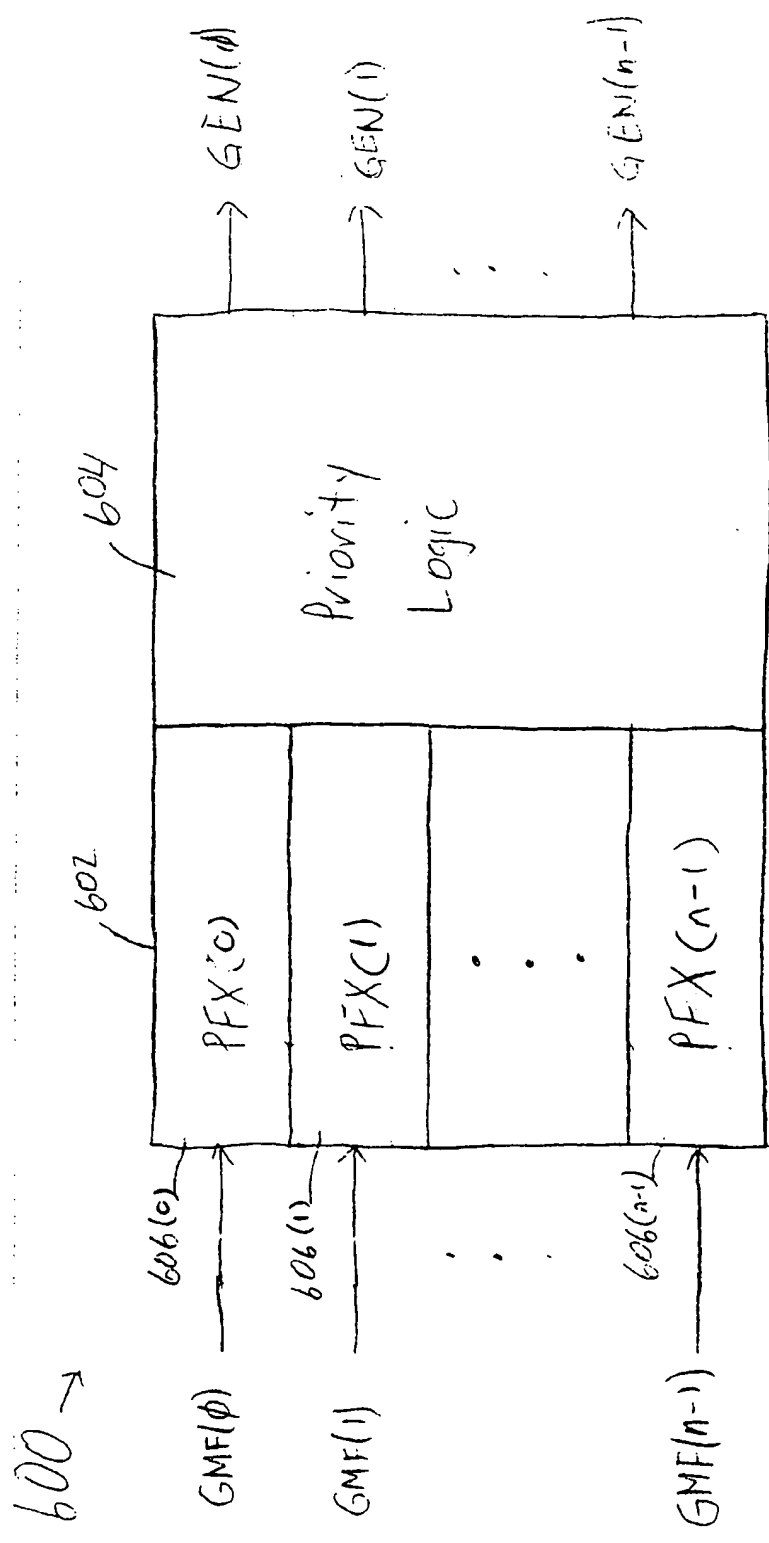
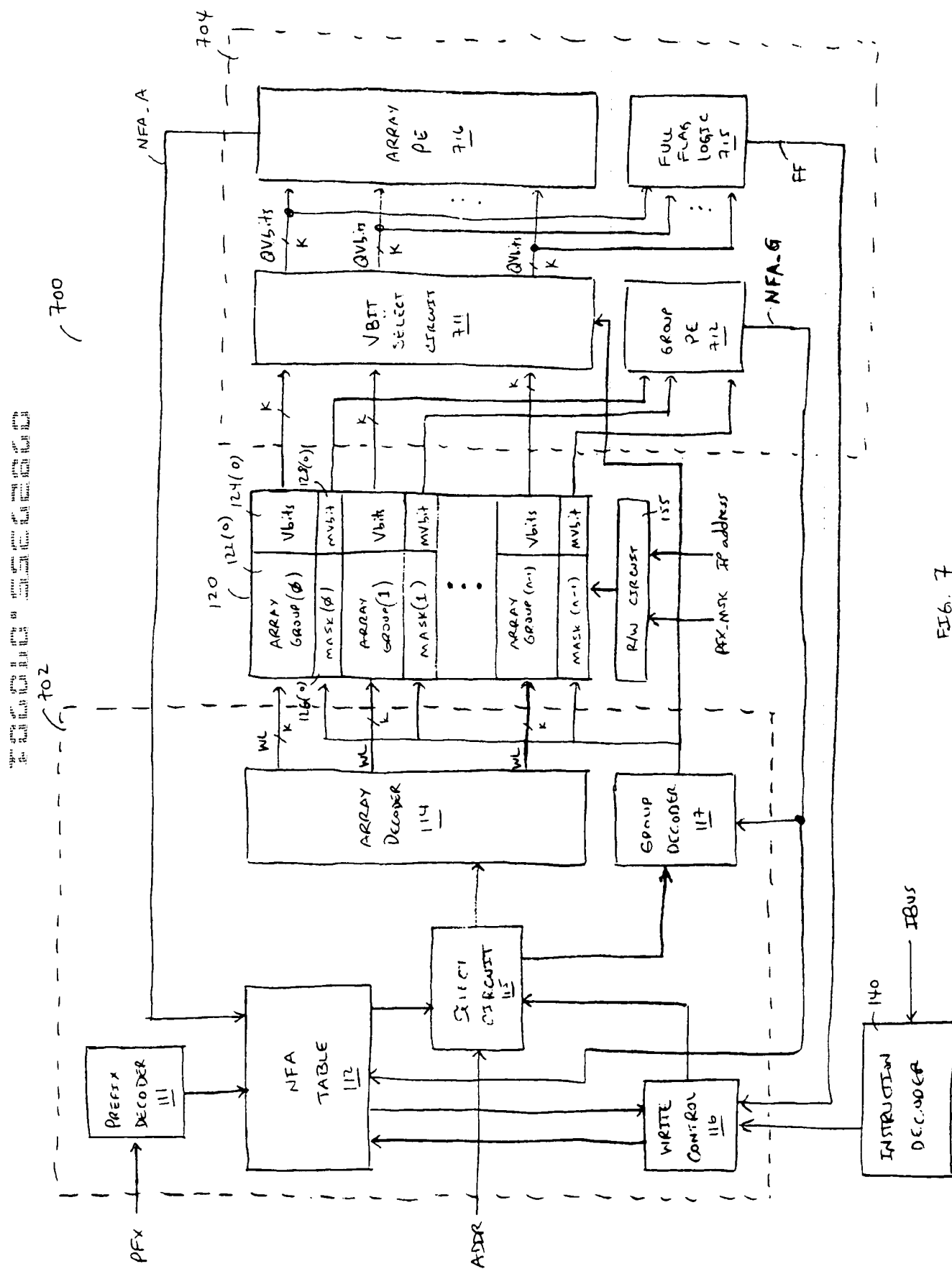


FIG. 6





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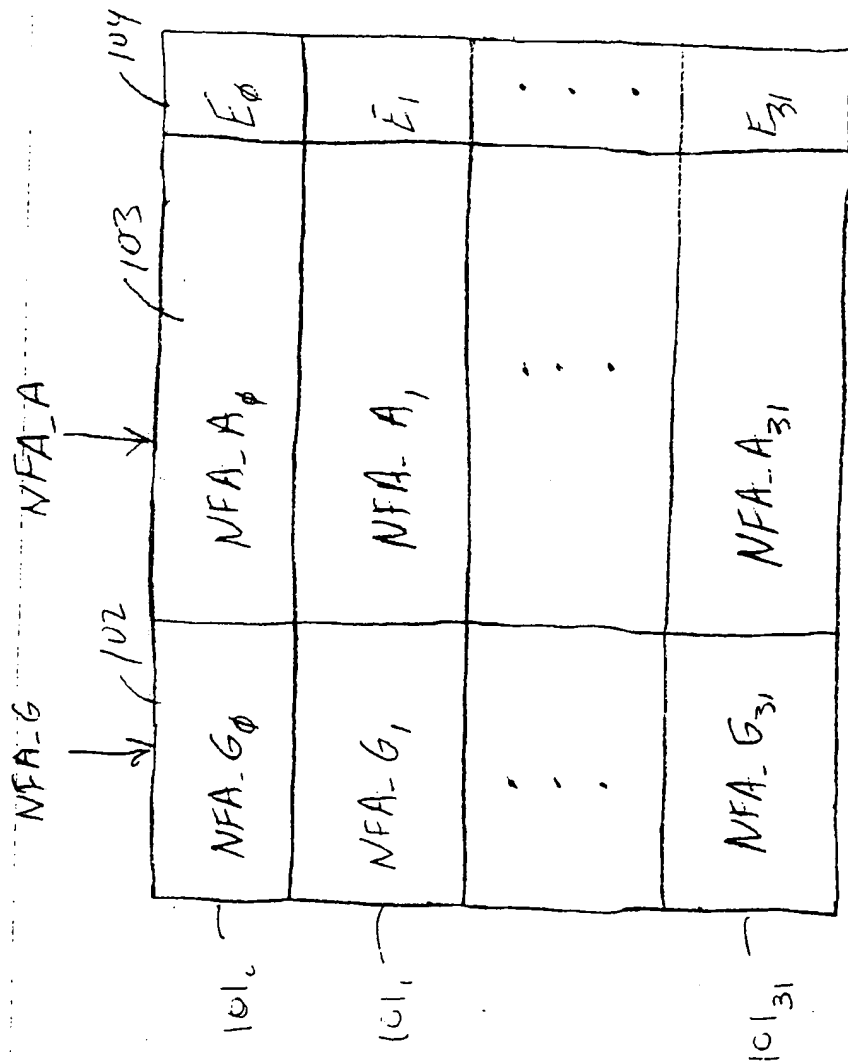


FIG. 8

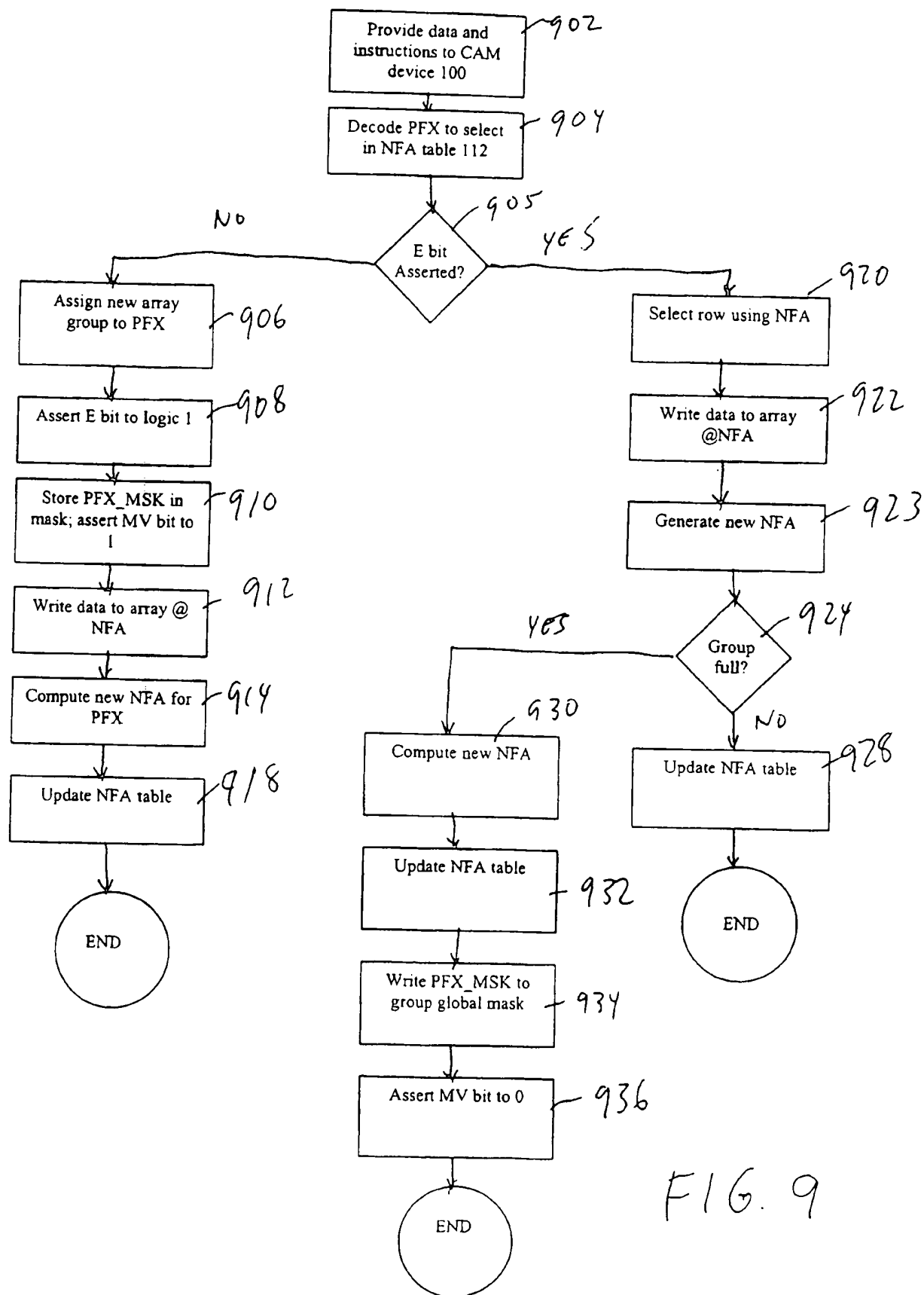


FIG. 9

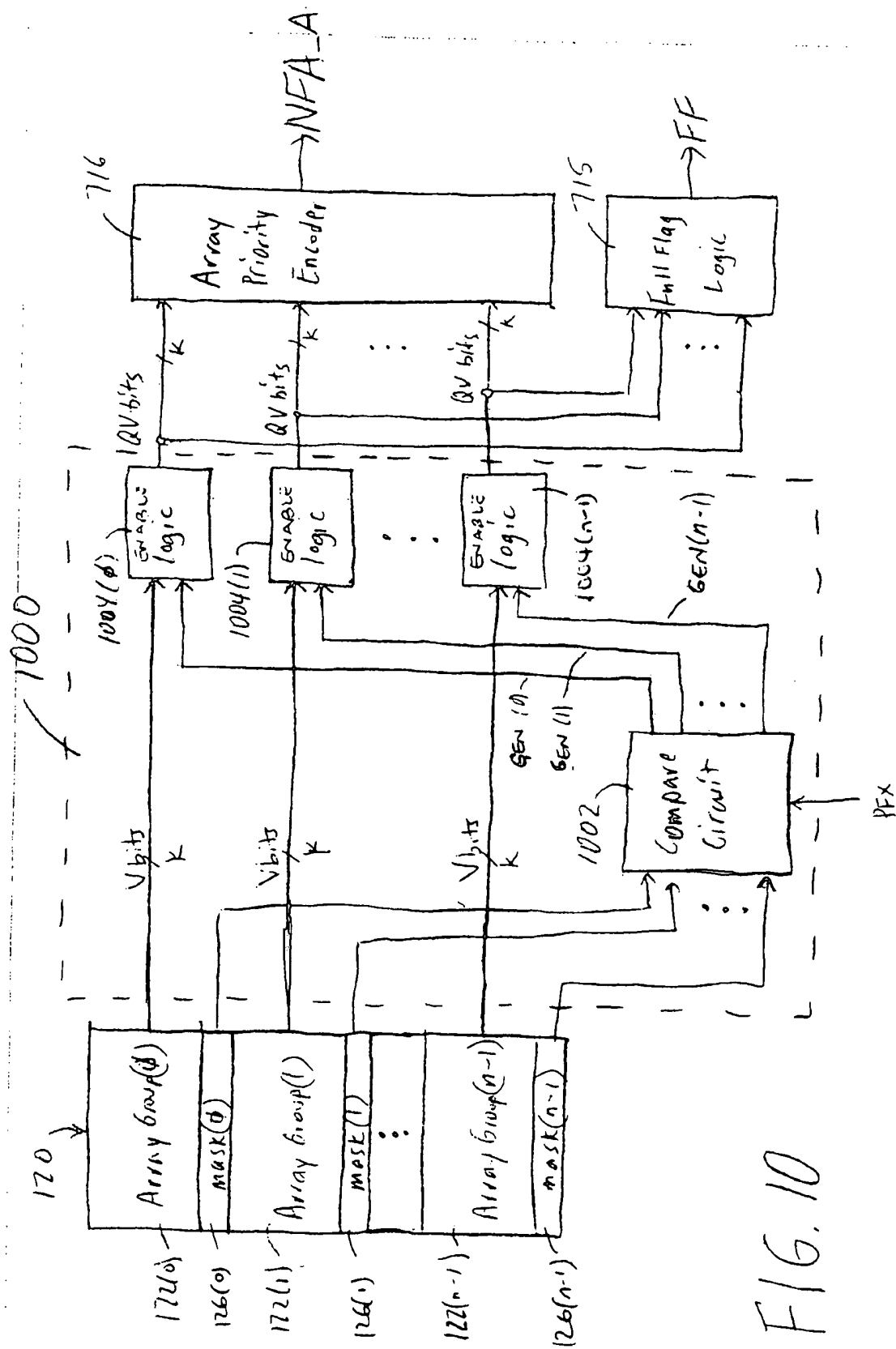


FIG. 11 is a block diagram of a parallel processing system. The system includes a plurality of parallel processing units, each receiving a common input and producing a common output. The units are connected to a common bus and a common output line.

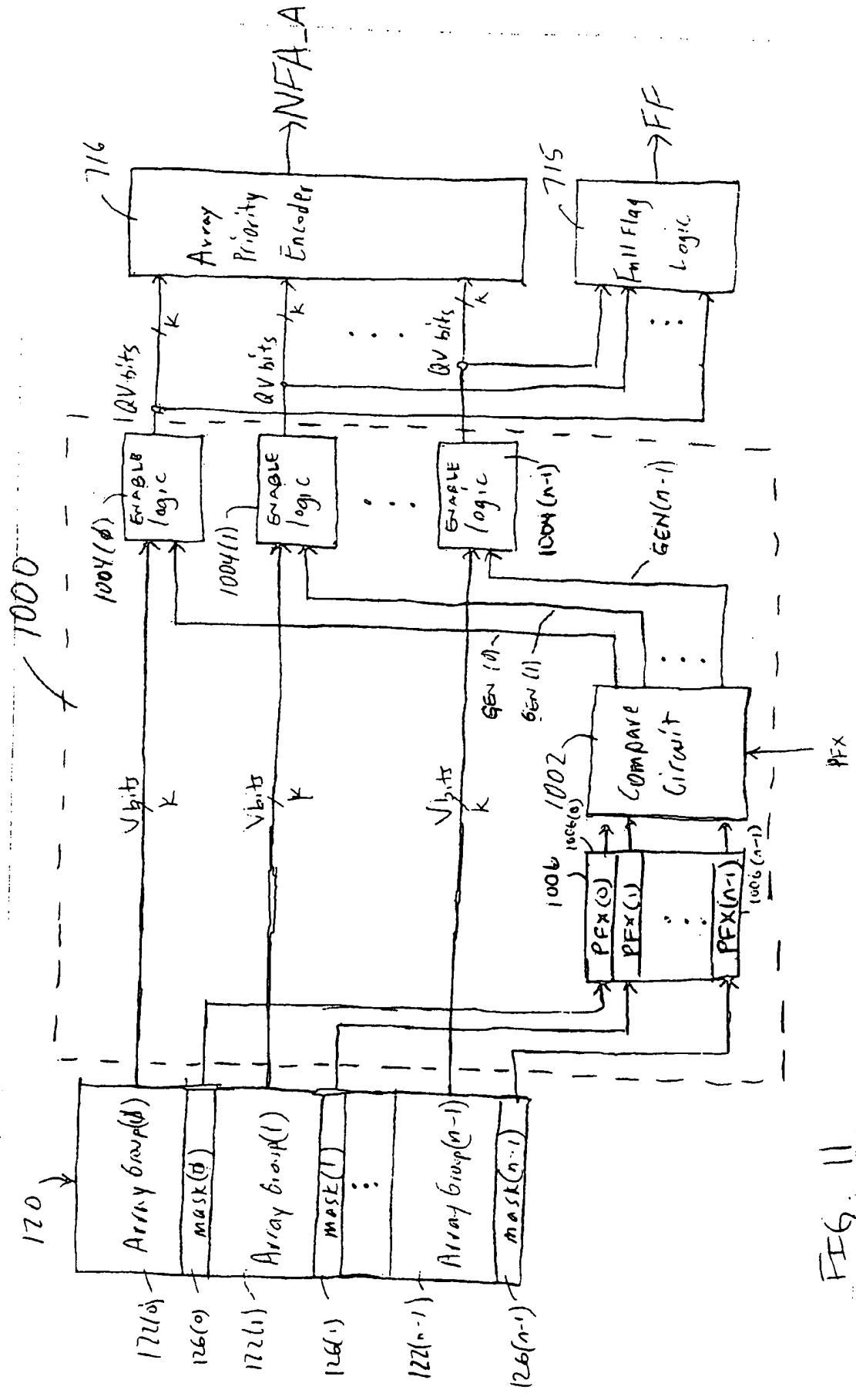


FIG. 11

